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APPLICATION PAPERS

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OF

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FOR

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TESTING MEMORY ACCESS SIGNAL CONNECTIONS

BACKGROUND OF THE INVENTION

5 ## Field of the Invention

This invention relates to data processing systems. More particularly, this invention relates to the testing of memory access signal connections between a data processing circuit and a memory coupled to that data processing circuit.

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Description of the Prior Art

It is known to provide testing mechanisms for testing integrated circuits when they have been manufactured to ensure that they operate correctly. One known

15 technique is to include serial scan chains into which test patterns, such as automatically generated test patterns (AGTPs), may be scanned in and result values scanned out to verify correct operation of the manufactured integrated circuits. As integrated circuits increase in complexity and have an increasing number of functional units embedded therein, the need for test in this way increases and the difficulty of

20 gaining access to deeply embedded portions of the integrated circuit with no direct connection to the external pins of the integrated circuit also increases. These problems are further compounded in that different functional elements within the integrated circuit may be designed and produced by different suppliers who may not release full details of the design of their functional unit as this is proprietary

25 information. This makes the design of appropriate test patterns to provide comprehensive test coverage more difficult.

In the above circumstances, one possibility is that the provider of the functional unit, such as a processor core, will also supply appropriate test patterns for

30 testing that functional unit when it is integrated within a larger integrated circuit (system-on-chip) design. Whilst this approach works well in many cases, a difficulty arises when the particular functional unit may be connected to a variety of different forms of additional circuitry which necessitate different test patterns to be used. In this context, the functional unit provider can try to produce a suite of test patterns to

cover all possible ways in which the functional unit may be used, but this is an onerous undertaking. As an example of this circumstance, a processor core may have a memory access port to which a memory of a variable size can be connected or optionally no memory at all connected. In order to test the memory access signal connections between the processor core and the memory, it would be possible to provide each of these signal connections with a scan chain cell such that test pattern data could be applied to and captured from these points. This would allow the connections to be tested without dependence upon the connected memory size. However, the memory access signal connections are often timing critical signal paths and the additional delay that may be introduced by inserting a multiplexer in these paths so as to accommodate a scan chain cell is a significant disadvantage. Furthermore, significant circuit area is consumed by scan chain cells and so it is desirable if possible to reduce these in number. It is known within test methodologies to control a data processing circuit with appropriately applied diagnostic signals such that it will exercise the memory access signal connections for a particular size of attached memory with the results of these stimulations being observed to ensure correct operation by checking the data fed back into the data processing circuit. However, such techniques are memory size specific and accordingly in order to deal with a variety of possible different memory sizes which may be attached, a disadvantageously large number of suitable test patterns need to be provided.

SUMMARY OF THE INVENTION

Viewed from one aspect the present invention provides a method of testing an apparatus for processing data having a memory operable to store data and a data processing circuit coupled to said memory via a memory access port having a plurality of memory access signal connections, said method comprising the steps of:

testing a subset of said plurality of memory access signal connections using respective associated diagnostic serial scan chain cells each operable to perform at least one of:

(i) applying a diagnostic signal value to a respective memory access signal connection of said subset; and

(ii) capturing a diagnostic signal value from said respective memory access signal connection of said subset; and

testing a remainder of said plurality of memory access signal connections by at least one of:

5   (iii) outputting a diagnostic signal generated by said data processing circuit to said memory from said data processing circuit via a respective memory access signal connection of said remainder; and

(iv) capturing with said data processing circuit a diagnostic signal input to said data processing circuit from said memory via a respective

10   memory access signal connection of said remainder.

The invention recognizes and exploits the feature that whilst memory size will vary (or a memory may not be present at all) and accordingly make some memory access signal connections optional or changed between different memory size

15 implementations, a large number of these memory access signal connections will remain unchanged. Thus, the system may be arranged to use scan chain cells on those memory access signal connections which are variable between different implementations to allow these to be separately tested by their own test pattern whereas the memory access signal connections which are common between different

20 implementations may be tested by being exercised by the data processing circuit concerned and the responses therefrom observed. In this way, there is a reduced requirement for scan chain cells in the integrated circuit as a whole and on the potentially timing limiting critical paths of the memory access signal connections. Furthermore, the number of different test patterns which need to be provided is

25 reduced to a more acceptable level.

In preferred embodiments of the invention, the subset of memory access signal connections which are provided with scan chain cells are ones from which diagnostic signal data is captured but does not need to be applied by scan chain cell mechanisms.

30 Scan chain cells which only capture data need not utilize a multiplexer in the critical data path so reducing the timing constraints which can be introduced by scan chain cell insertion. Memory access signal connections of the type from which data is normally only required to be captured include memory address signal connections.

These are of the type which tend to be optionally used and present depending upon memory size used, which is one of the major variables in the form of the overall integrated circuit.

5   The provision of serial scan chain cells is not however limited to such memory address signal lines, as there are other signal lines which may optionally be present, which are not timing critical and which may be used with serial scan chain cells which apply diagnostic signals rather than merely capture diagnostic signals.

10   It will be appreciated that the data processing circuit coupled to the memory could take a wide variety of different forms, such as a digital signal processor, a data engine or the like. However, the present technique is particularly well suited to embodiments in which the data processing circuit is a processor core.

15   Similarly, it will be appreciated that the memory coupled to the data processing circuit could take a variety of forms such as a main memory, a cache memory or the like. However, the present technique is particularly well suited to situations in which the memory is a tightly coupled memory.

20   The testing of the remainder of the memory access connections with data driven out to and captured back from the memory is facilitated by manipulating one or more memory size signals which indicate the size of the memory that is present. The memory may have a range of optional sizes, but this type of testing, and the consequent need for an appropriate test pattern, can be restricted to the smallest non-
25 zero memory size that is supported. The memory size signals are changed, possibly using pin signals, but preferably using serial scan chain derived signals, to specify a smaller memory than is in reality present. The non-scan cell testing can then be restricted to the smaller memory size.

30   Viewed from another aspect the present invention provides apparatus for processing data, said apparatus comprising:

a memory operable to store data; and

a data processing circuit coupled to said memory via a memory access port having a plurality of memory access signal connections; wherein

a subset of said plurality of memory access signal connections have respective associated diagnostic serial scan chain cells operable to perform at least one of:

applying a diagnostic signal value to a respective memory access signal connection; and

capturing a diagnostic signal value from said respective memory access signal connection; and

a remainder of said plurality of memory access signal connections do not have respective associated diagnostic serial scan chain cells.

The above, and other objects, features and advantages of this invention will be apparent from the following detailed description of illustrative embodiments which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 schematically illustrates a processor core coupled via a memory access port to a memory;

Figure 2 schematically illustrates the system of Figure 1 in more detail showing the different test treatment of different portions of the memory access port;

Figure 3 schematically illustrates two different types of scan chain cell which may be used on memory access signal connections in accordance with the present technique; and

Figure 4 is a flow diagram schematically illustrating a test methodology utilizing the present techniques.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a portion of an integrated circuit including a processor core 2 and a memory 4. Combinatorial logic within the processor core 2 is connected to the memory access port 6 and does not connect to other portions of the system to enable it to be otherwise tested. The memory 4 can vary in size depending upon the particular

5 requirements of the system concerned (in some systems no memory may be present) and such variation in size can have an impact upon the precise form of the memory access port 6 and the memory access signal connections utilized. Accordingly, running a test operation upon the processor core 2 to exercise the memory access port 6 does not enable different sizes of memory 4 to be tested and would require different test pattern

10 sets to be generated to stimulate the processor core 2 appropriately so as to accommodate all the different memory sizes possible for the memory 4. Memory size signals, which are usually tied during instantiation of a particular integrated circuit, are used to specify which particular optional memory size is present.

15 Figure 2 illustrates the system of Figure 1 in more detail, but in this case the memory access signal connections between the processor core 2 and the memory 4 are divided into a subset 8 which are provided with respective serial scan chain cells 10 and a remainder 12 which are tested by diagnostic signals driven out from the processor core 2 or captured back by the processor core 2. The remainder portion 12 is thus tested by

20 signals driven through the memory 4 rather than relying upon the capabilities of serial scan chain cells 10 which can test these connections without requiring the memory 4 itself to participate in the testing operation. The remainder portion 12 corresponds to the smallest supported non-zero memory size as specified by changed memory size signals used during testing. These changed memory size signals are derived from scan cell

25 signals input during test and used to override the true memory size signals specifying the operational memory size for use during non-test operation. Thus, as part of enabling only the remainder portion 12 to require a test pattern, the integrated circuit is supplied with memory size signals specifying a smaller memory than is actually present and one for which the memory access connections may be tested using the single (or small

30 number) of test pattern that need be provided.

The subset of memory access signal connections 8 which are provided with serial scan chain cells 10 typically includes the high order memory address signal lines as these

are ones which tend optionally to be used depending upon the memory size of the memory 4 being employed by a particular implementation. Accordingly, taking the variability of the use or non-use of these high order memory address signal lines out of the factors controlling the need to provide different test patterns reduces the number of

5   test patterns required. Certain control signals which form part of the memory access signal connections may also be subject to optional use depending upon the type of memory 4 being used or the size of the memory 4 being used. These control signals could also be supplied with a suitable scan chain cell for direct testing.

10   The high order memory address signal lines are such that it is normally only desired to test data being driven out to these lines. Indeed, in normal operation the signal flow is normally always from the processor core 2 to the memory 4 for memory address signal lines.

15   Figure 3 schematically illustrates two scan chain cell arrangements which may be used with the subset of connections for which scan chain cells are provided. The upper example is a non-registered memory address port signal line from which it is only desired to capture diagnostic signals generated by the functional logic 14 within the processor core 2. This may be achieved with a scan chain cell 16 having an input

20   selectively connected to the memory address port signal line without requiring a multiplexer to be inserted into that signal line functional path. The lower example is of a registered memory address port signal line. The register 18 for such a registered signal line can be reused as the serial scan chain cell for diagnostic purposes.

25   Figure 4 is a flow diagram schematically illustrating a testing methodology for the system of Figure 2. At step 20 a test pattern is loaded using a serial scan chain (such as the wrapper scan chain) to test the processor core 2 and those memory port connections 8 which are provided with scan chain cells, e.g. high order address bits of the memory access port connecting to the optional memory. The memory size signals

30   are also toggled during this testing to check these signals. The memory port connections with scan cells are tested by driving signals out of the processor core 2 for capture in the scan chain cells 10 under the test pattern control. Step 22 serves to determine whether or not this phase of the testing is passed. If the test is not passed, then processing

proceeds to step 23 at which the component is failed. If the check for a pass at step 22 is successful, then processing proceeds to step 24 at which an appropriate test pattern is driven into the processor core 2 to test the remaining memory access port connections (if a memory is actually connected) by driving signals out of the processor core 2, through

5   the memory 4 and back into the processor core 2 under test pattern control. Whilst this testing is taking place the memory size signals are set to have values such that the memory (if present) is taken to have the smallest non-zero supported memory size. Step 26 then determines whether or not this test has been passed. If the test has not been passed, then the component is again failed at step 24. If the test at step 26 indicates a

10   pass of the second phase of the testing, then processing proceeds to step 28 at which the component concerned is passed and maybe released for use. If an optional memory is not present the steps 24 and 26 can be omitted.

Although illustrative embodiments of the invention have been described in detail herein with reference to the accompanying drawings, it is to be understood that the

15   invention is not limited to those precise embodiments, and that various changes and modifications can be effected therein by one skilled in the art without departing from the scope and spirit of the invention as defined by the appended claims.